

# GL553VD Block Diagram

**REV 2.0**

## Power

+VCORE  
+VCCGT  
+VCCSA

System (5V & 3.3V)

1.0VSUS

DDR & VTT

1V8\_VGA\_N17

BATTERY CHARGER

VCCIO

LOAD SWITCH

Power Protect

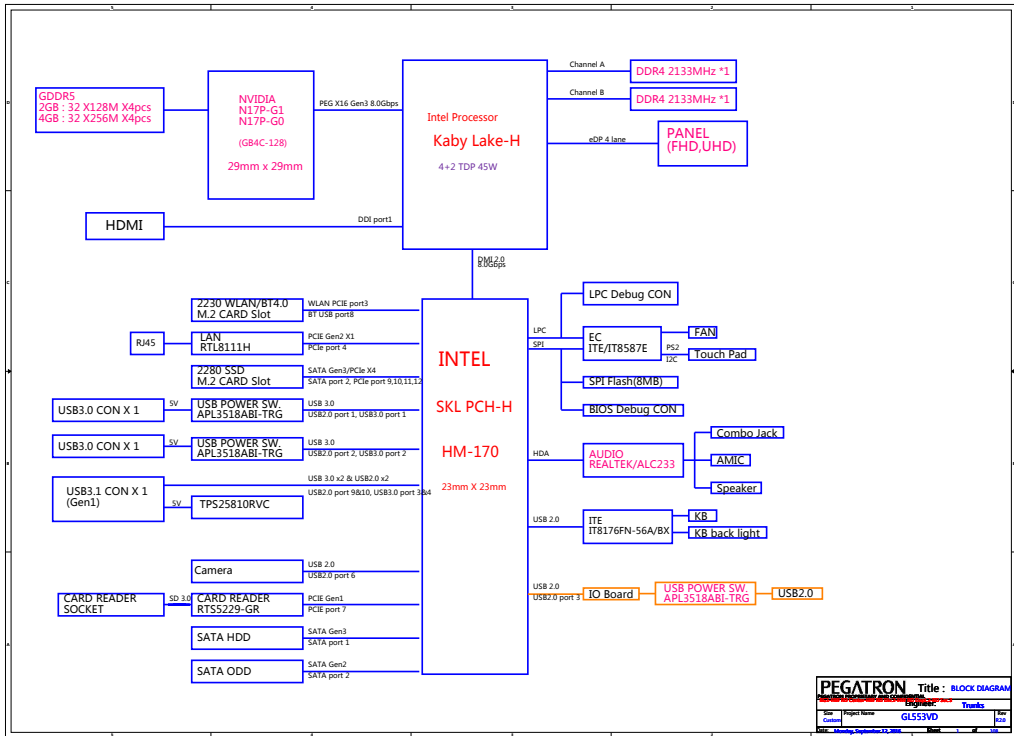
1.0VS\_VGA

+VGA\_VCORE

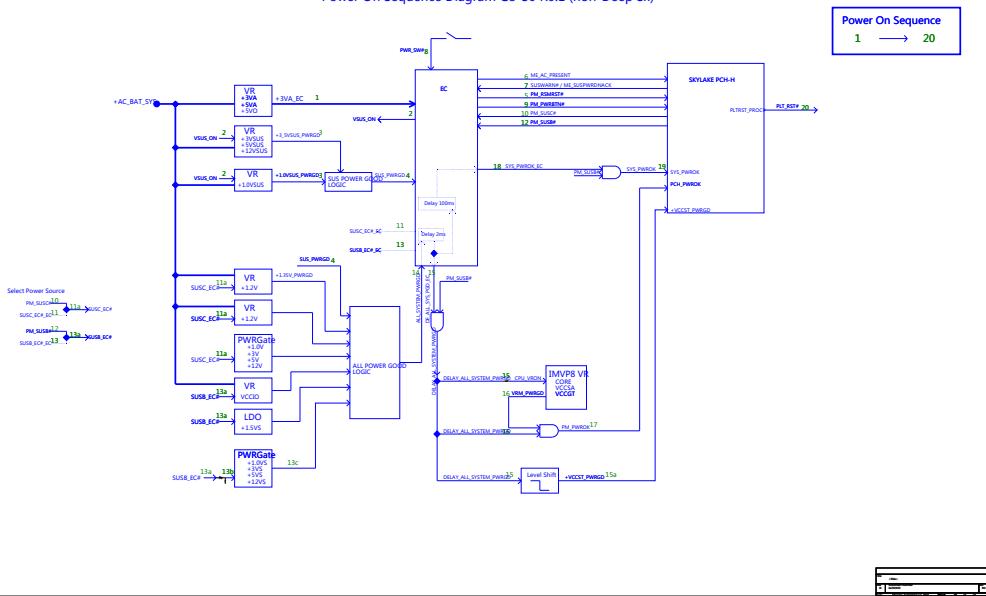
+2P5VPP

+FBVDDQ

+NVVDDS\_N17

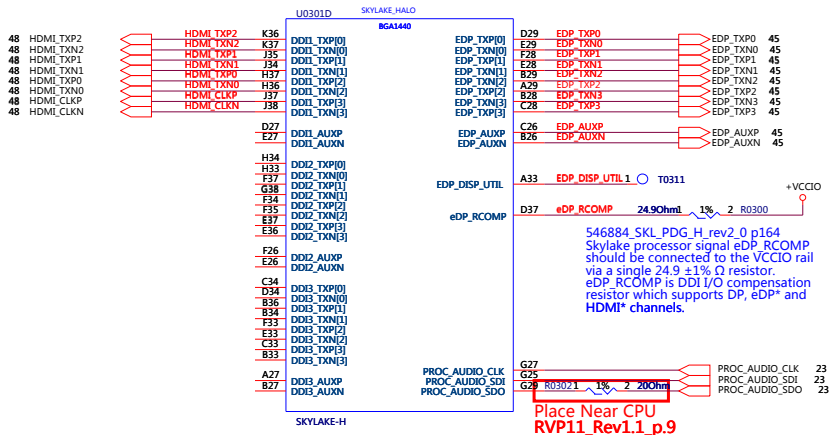


### Power On Sequence Diagram G3-S0 R0.1 (non-Deep Sx)



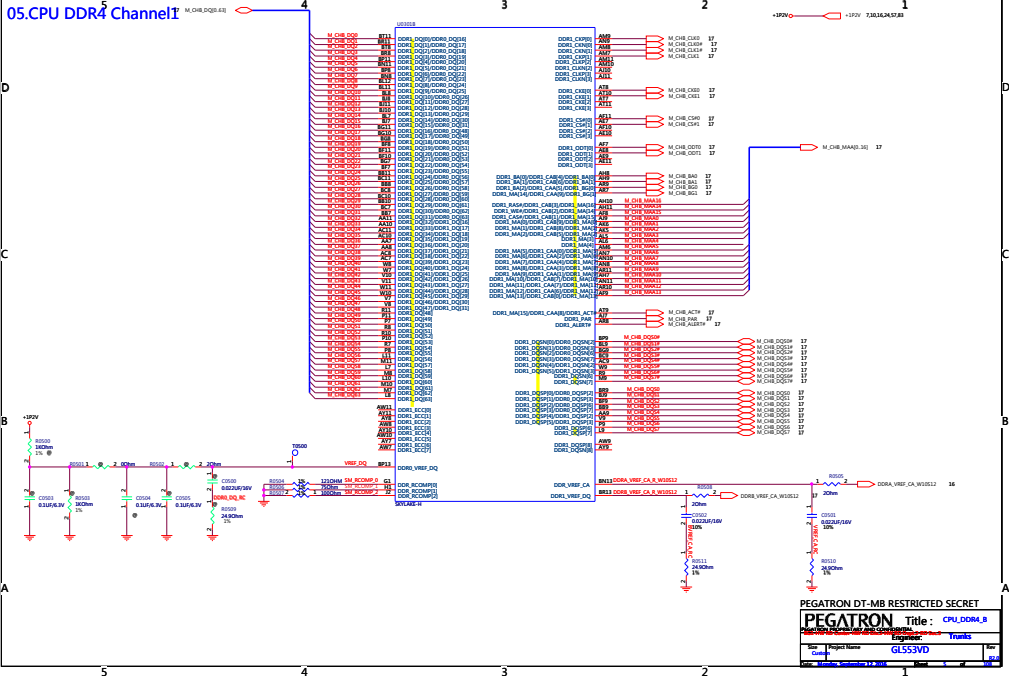


### 3.CPU\_DDI/EDP





## 05.CPU DDR4 Channel1



# 06.CPU DMI/PEG

70 PCIEB\_R0XN[15:0]  
70 PCIEB\_R0XP[15:0]

PCIEG\_TXN[15:0]  
PCIEG\_TXP[15:0]

PEG Lane reversal

+VCCIO R0600 1 1% 2 24.9Ohm PEG\_RCOMP 62  
NOTE:  
W/S=12/15 mil, length<400mil

20 DMI\_R0XP0  
20 DMI\_R0XN0  
20 DMI\_R0XP1  
20 DMI\_R0XN1  
20 DMI\_R0XP2  
20 DMI\_R0XN2  
20 DMI\_R0XP3  
20 DMI\_R0XN3

U0301C

PCIEB\_R0XP15 E25  
PCIEB\_R0XN15 D25  
PCIEB\_R0XP14 E24  
PCIEB\_R0XN14 D24  
PCIEB\_R0XP13 E23  
PCIEB\_R0XN13 D23  
PCIEB\_R0XP12 E22  
PCIEB\_R0XN12 D22  
PCIEB\_R0XP11 E21  
PCIEB\_R0XN11 D21  
PCIEB\_R0XP10 E20  
PCIEB\_R0XN10 D20  
PCIEB\_R0XP9 E19  
PCIEB\_R0XN9 D19  
PCIEB\_R0XP8 E18  
PCIEB\_R0XN8 D18  
PCIEB\_R0XP7 E17  
PCIEB\_R0XN7 D17  
PCIEB\_R0XP6 E16  
PCIEB\_R0XN6 D16  
PCIEB\_R0XP5 E15  
PCIEB\_R0XN5 D15  
PCIEB\_R0XP4 E14  
PCIEB\_R0XN4 D14  
PCIEB\_R0XP3 E13  
PCIEB\_R0XN3 D13  
PCIEB\_R0XP2 E12  
PCIEB\_R0XN2 D12  
PCIEB\_R0XP1 E11  
PCIEB\_R0XN1 D11  
PCIEB\_R0XP0 E10  
PCIEB\_R0XN0 D10  
PEG\_R0XP[0]  
PEG\_R0XN[0]  
PEG\_R0XP[1]  
PEG\_R0XN[1]  
PEG\_R0XP[2]  
PEG\_R0XN[2]  
PEG\_R0XP[3]  
PEG\_R0XN[3]  
PEG\_R0XP[4]  
PEG\_R0XN[4]  
PEG\_R0XP[5]  
PEG\_R0XN[5]  
PEG\_R0XP[6]  
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PEG\_R0XP[12]  
PEG\_R0XN[12]  
PEG\_R0XP[13]  
PEG\_R0XN[13]  
PEG\_R0XP[14]  
PEG\_R0XN[14]  
PEG\_R0XP[15]  
PEG\_R0XN[15]

PEG\_RCOMP

SKYLAKE-H

PEG\_TXP[0]  
PEG\_TXN[0]  
PEG\_TXP[1]  
PEG\_TXN[1]  
PEG\_TXP[2]  
PEG\_TXN[2]  
PEG\_TXP[3]  
PEG\_TXN[3]  
PEG\_TXP[4]  
PEG\_TXN[4]  
PEG\_TXP[5]  
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PEG\_TXN[11]  
PEG\_TXP[12]  
PEG\_TXN[12]  
PEG\_TXP[13]  
PEG\_TXN[13]  
PEG\_TXP[14]  
PEG\_TXN[14]  
PEG\_TXP[15]  
PEG\_TXN[15]

DMI\_TXP0  
DMI\_TXN0  
DMI\_TXP1  
DMI\_TXN1  
DMI\_TXP2  
DMI\_TXN2  
DMI\_TXP3  
DMI\_TXN3

Title : CPU\_DMI

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Engineer: Trunks

Size A4 Project Name GL553VD Rev R20

Date: Monday, September 12, 2016 Sheet 6 of 108

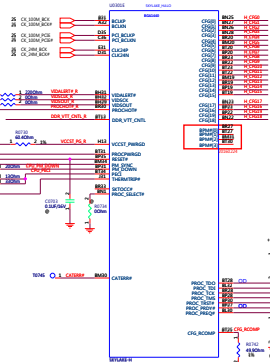
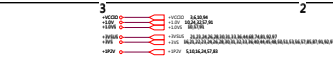
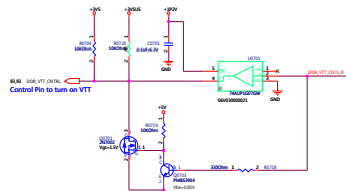
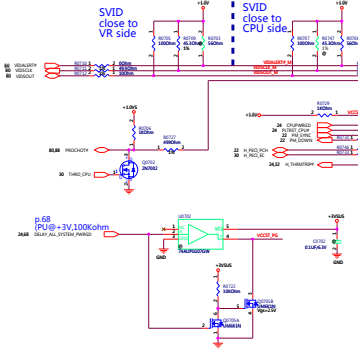
# 07.CPU MISC

Table 12-16-SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3+W4+W5+W6 [inches]	W7 [inches]	W8 [inches]	R101 [Ω]	R102 [Ω]	R103 [Ω]	R104 [Ω]	W105 [Ω]
VSVIDOUT	0.5-1	1-1.5	0.5-4	0-1.7	<0.1	<0.1	100	100	0	30
VSVIDOR						Empty	40	0	30	1.0
VSVIDENBT #							56	220	0	

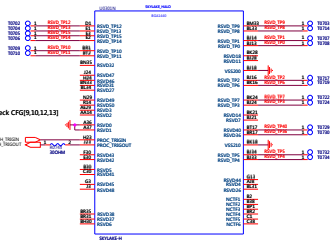
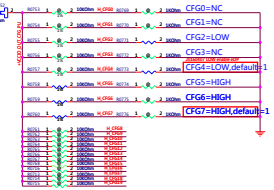
SVID  
close to  
VR side

SVID  
close to  
CPU side.



Check CFG [2][5][6] for PEG  
bifurcate setting

Signal	W1 [inches]	W2 [inches]	W3+W4+W5+W6 [inches]	W7 [inches]	W8 [inches]	R101 [Ω]	R102 [Ω]	R103 [Ω]	R104 [Ω]	W105 [Ω]
VSVIDOUT	0.5-1	1-1.5	0.5-4	0-1.7	<0.1	<0.1	100	100	0	30
VSVIDOR						Empty	40	0	30	1.0
VSVIDENBT #							56	220	0	



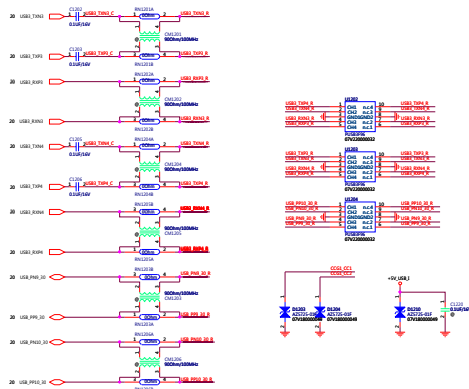
Check CFG[9,10,12,13]





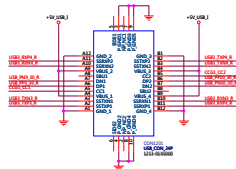


## 12. Type-C (CC logic, Conn.)



### Type-C Conn.

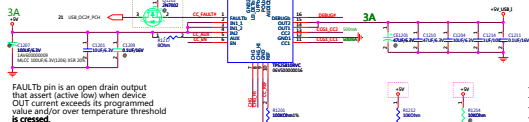
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D1+	D1-	SBU+	Vbus	RX2+	RX2-	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
GND	RX1+	RX1-	Vbus	SBU+	D2+	D2-	CC2	Vbus	TX2+	TX2-	GND



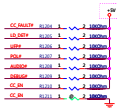
### CC logic

Leads to PCH+ (Vbus\_ORG) to CC1+5V)

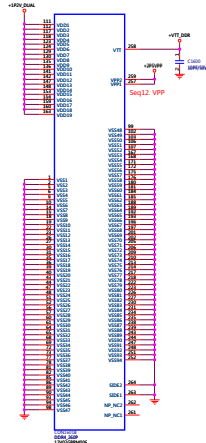
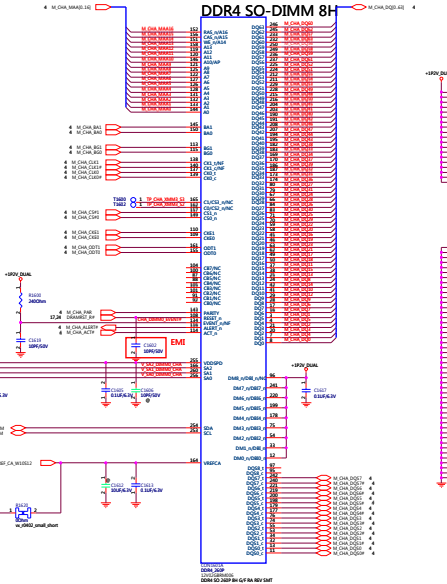
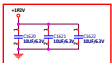
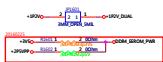
ChG	ChG_L	CC Capability	Connect USB	Load Detect Threshold
0	0	STD	1.57A	NA
0	1	STD	1.57A	NA
1	0	1.5A	1.57A	NA
1	1	3.0A	3.34A	1.77A



FAULTb pin is an open drain output that asserts (active low) when device OUT current exceeds its programmed value and/or over temperature threshold is crossed.



## 16.DDR4\_SO-DIMM0

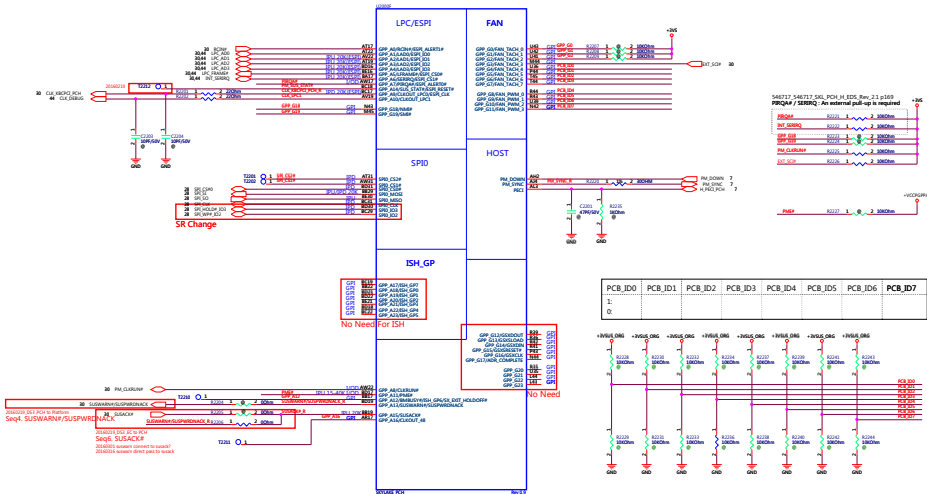








+VDD5 0 7 14 21 28 35 42 49 56 63 70 77 84 91 98 105 112 119 126 133 140 147 154 161 168 175 182  
 +VDD5 0 1 8 15 22 29 36 43 50 57 64 71 78 85 92 99 106 113 120 127 134 141 148 155 162 169 176 183  
 +VDD5 0 2 9 16 23 30 37 44 51 58 65 72 79 86 93 100 107 114 121 128 135 142 149 156 163 170 177 184  
 +VDD5 0 3 10 17 24 31 38 45 52 59 66 73 80 87 94 101 108 115 122 129 136 143 150 157 164 171 178 185



PCB_ID0	PCB_ID1	PCB_ID2	PCB_ID3	PCB_ID4	PCB_ID5	PCB_ID6	PCB_ID7
1:							
0:							



## 23.PCH\_AUDIO/CLK/I2C/UART





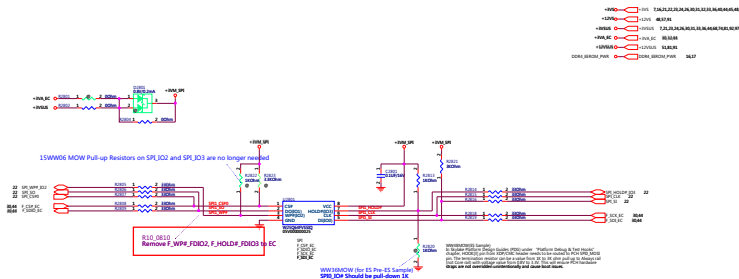






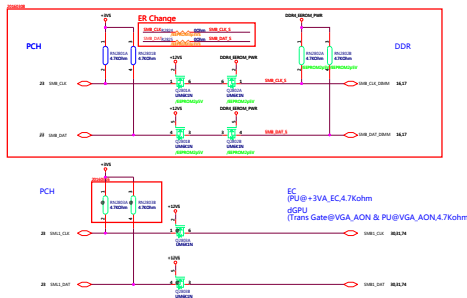
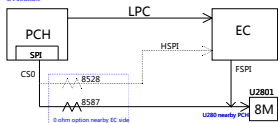
## 28.SPI ROM/Smbus

### SPI ROM

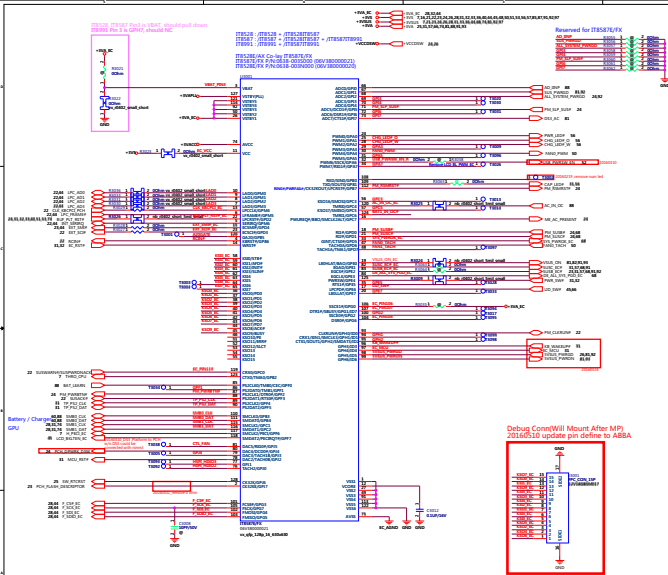


### SMBus

EC co-lay 8528/8587  
S/N Structure



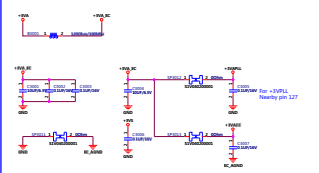
DRIVER: CHRG Pin is BAT+, should put down  
 REVERSE Pin is GND, should NC



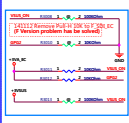
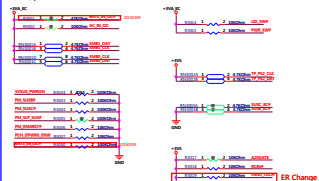
Debug Conn(Will Mount After MPI  
 20160510 update pin define to A88A



### For EC Power



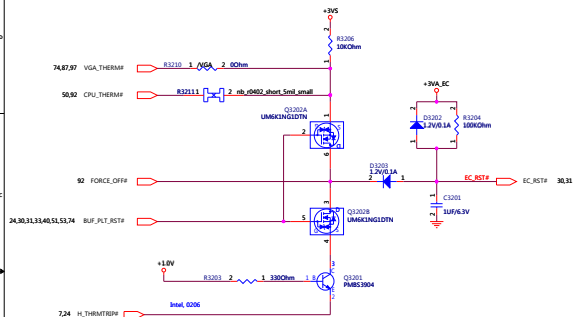
### For PU / PD



ES.0 PCH internal pull high (that is no weak)  
 ES.1.1112 Change Option Mask  
 for weak voltage at beginning of AC plug-in

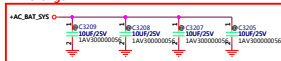


## 32. RST Circuit

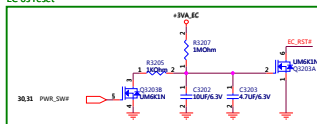


+3V5\_EC 3V5\_EC 28,30,44  
 +3V5 7,16,21,22,23,24,26,28,30,31,33,36,40,44,45,48,50,51,53,56,57,85,87,91,92,97  
 +1.0V 7,10,24,57,91

### ER Change

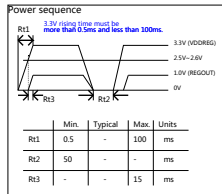
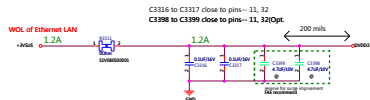
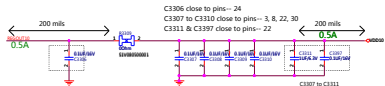
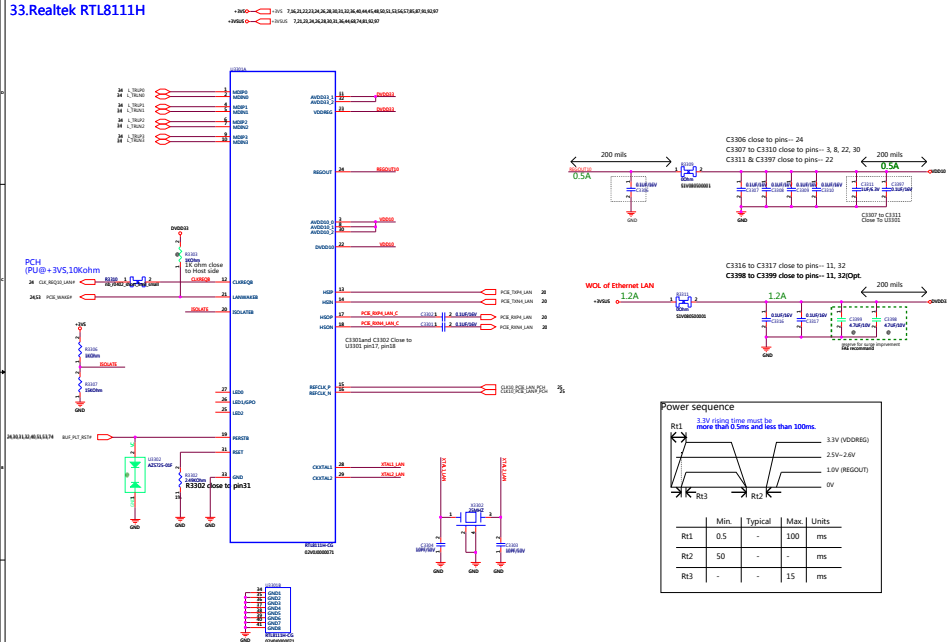


### EC 6s reset

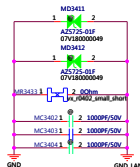
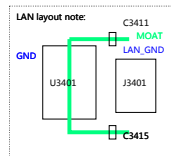
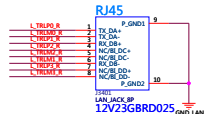
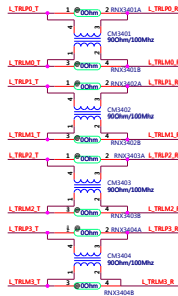
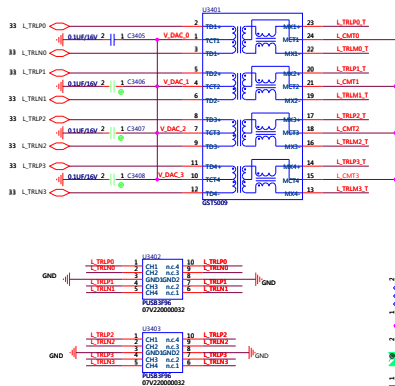


<b>PEGATRON</b>		Title: 32. RST Circuit	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BGL-HW RD Center-HW RD Dlx-2-HW RD S&M			
Size		Project Name	
8		GL553VD	
Date: 2023/09/26 14:00:00		Drawn	22 of 100

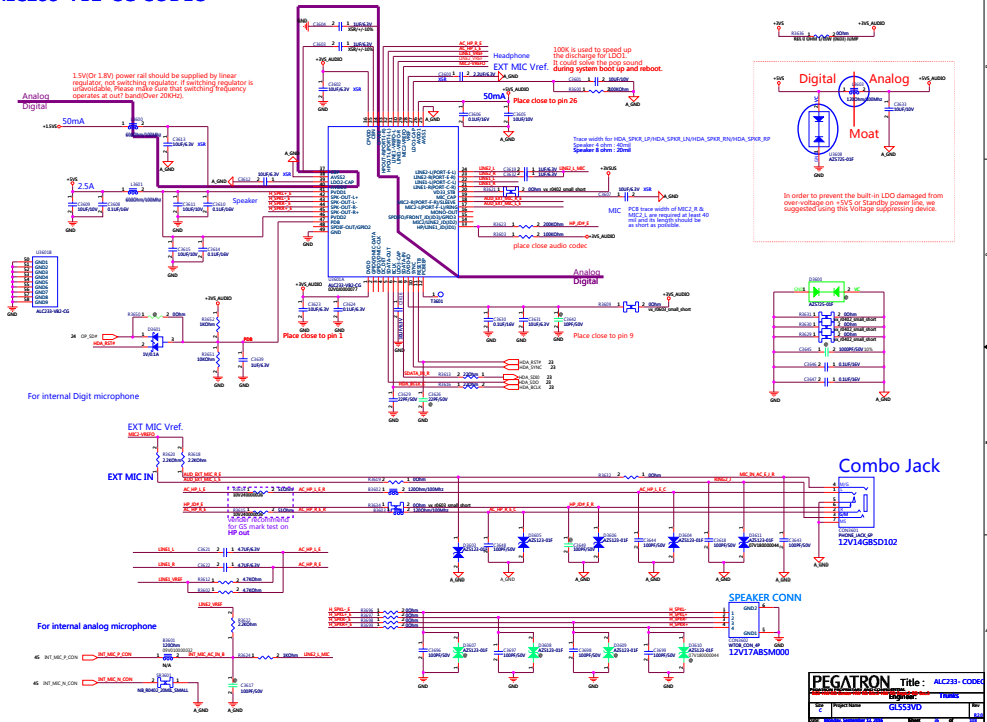
### 33.Realtek RTL8111H



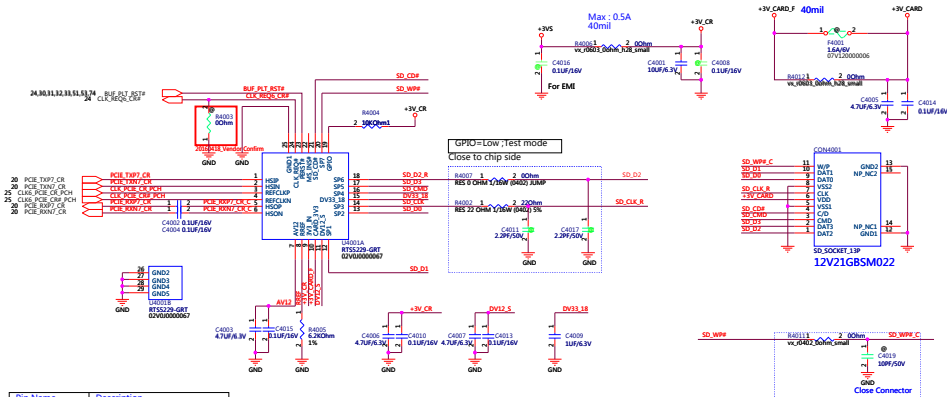
## 34. Transformer/RJ45



# ALC233-VB2-CG CODEC



## Cardreader



Pin Name	Description
SP1	SOWP# / MCLK
SP2	MS_IN#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_B5



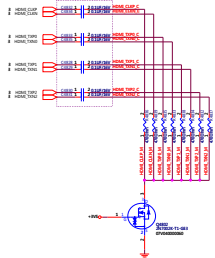


# HDMI

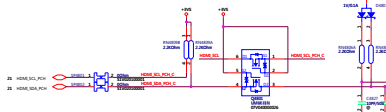
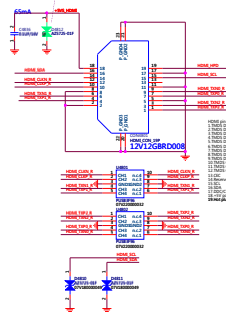
Eleto-XTechnical

R10\_0727\_EMI  
Impedance 85ohm

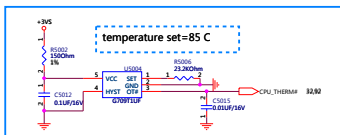
R11\_1007\_EMI  
Impedance modify to 85ohm



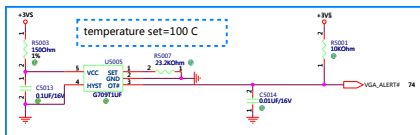
R10\_2160316\_EMI Reserve



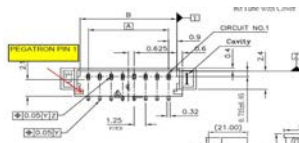
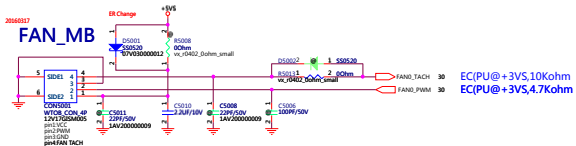
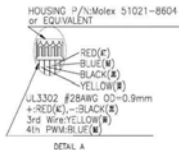
## CPU Thermal Sensor



## GPU Thermal Sensor



## FAN\_Module



<b>PEGATRON</b>		Title :	FAN/THERMAL
PEGATRON PROPERTY AND CONFIDENTIAL		Engineer :	Trunks
Rev :	Project Name :	GL553VD	Rev :
Date :	Issued :	Supervisor :	Rev :

NGFF socket M  
PCIEx4 SSD1

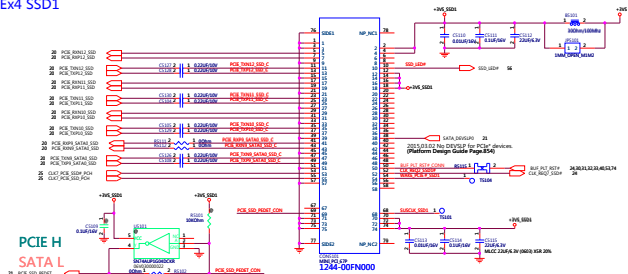
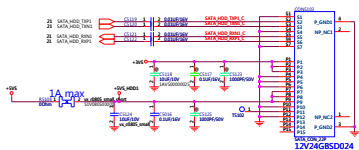


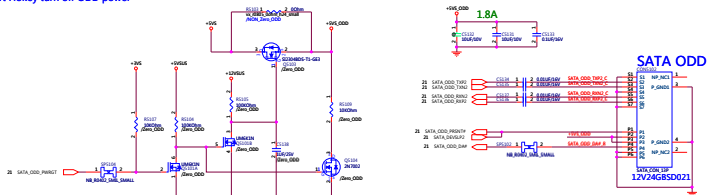
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

[illegible]

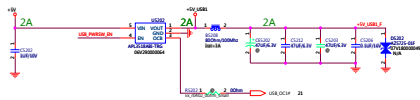
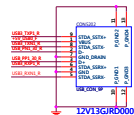
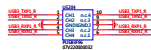
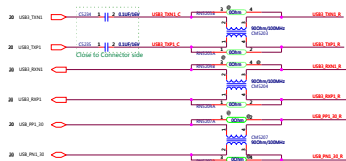
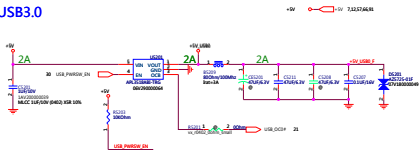
SATA HDD



support Hokey turn off ODD power



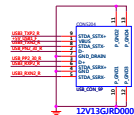
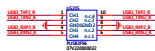
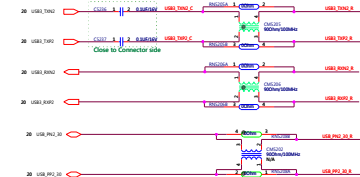
## 52.USB3.0



PLACE ESD Diodes near Connector



PLACE ESD Diodes near Connector



PEGATRON CY-MR-RESTRICTED SECRET

PEGATRON Title : USB3 Port

Project Name GL553VD

Rev: 1.0

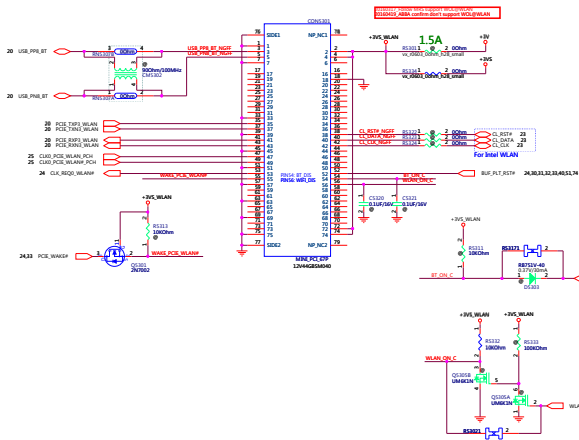
Author: [Name]

Check: [Name]

Date: [Date]

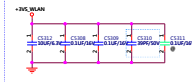
+2V  +2V 24,45,57,68,91

NGFF 2230 Key A\_slot A(WIFI)



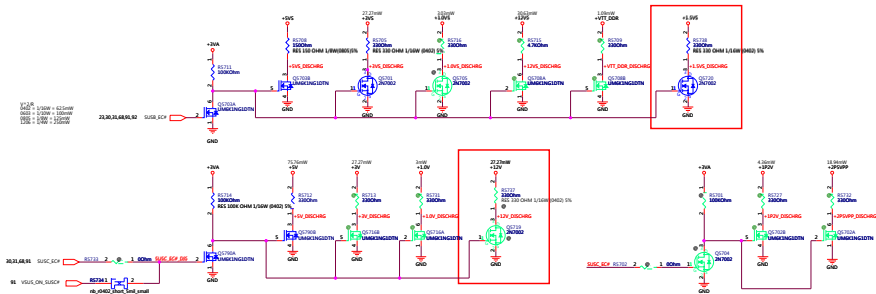
## WLAN+BT

**WLAN +3VS bypass capacitor:**  
Place 0.1uF near pin 2,24,52,39 41(CON5301).  
Place 10uF near +3VS\_WLAN source side.



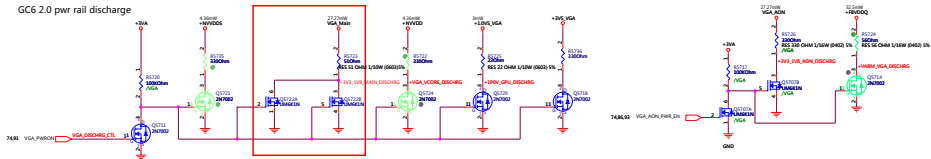


$V_{DD} = 0V$   
 $Q_{D1} = 1.20W + 0.20W$   
 $Q_{D2} = 1.20W + 0.20W$   
 $Q_{D3} = 1.20W + 0.20W$   
 $Q_{D4} = 1.20W + 0.20W$



all MOS pwr for GPU Optimus function

CG6 2.0 pwr rail discharge

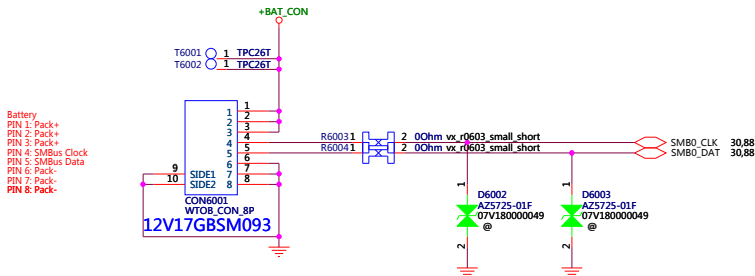


PEGATRON DT-MR-RESTRICTED SECRET

PEGATRON		Title: Discharge
Engineer		Thanks
Rev	Project Name	GL553VD
Rev	Rev	Rev

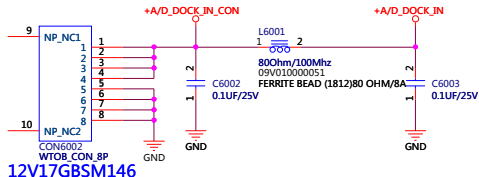
# 60.BATT CON/AC IN

## BATTERY CONNECTOR



## AC IN CONNECTOR

Adaptor  
120W

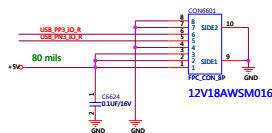
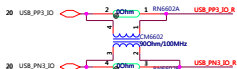


<b>PEGATRON</b>		Title :	BATT CON/AC IN
PEGATRON PROPRIETARY AND CONFIDENTIAL DSCT-11W-R0-Center-11W-R0-Div2-11W-R0-Rev2-2-R0-Sec3			
Engineer:		Trunks	
Size A	Project Name	GL553VD	Rev R2.0

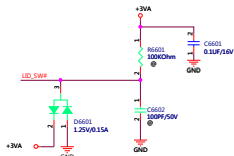
Date: Monday, September 12, 2016 Sheet 60 of 108

# IO BD CONN. (MB SIDE)

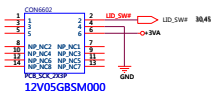
+5V 7,12,52,57,91  
+3VA 25,30,31,57,74,81,88,91,93



# Hall sensor Conn. (MB SIDE)



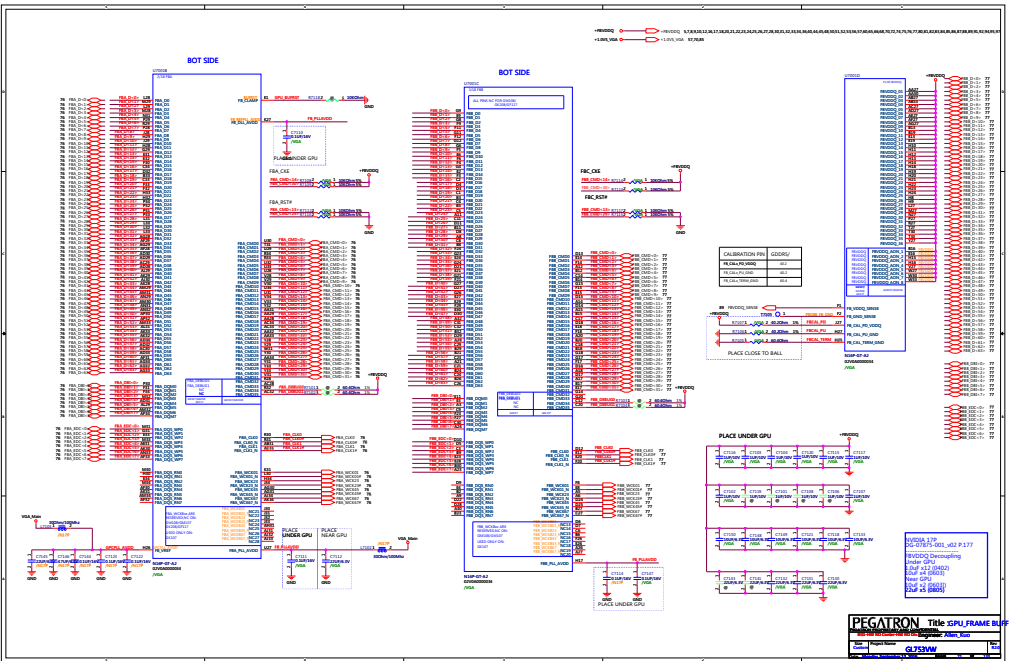
CON6602  
pin1: LID\_SWF\_H  
pin2: LID\_SWF\_H  
pin3: GND\_H  
pin4: +3VA\_H  
pin5: +3VA\_H  
pin6: +3VA\_H  
pin7: +3VA\_H  
pin8: +3VA\_H  
pin9: +3VA\_H  
pin10: +3VA\_H  
pin11: +3VA\_H  
pin12: +3VA\_H  
pin13: +3VA\_H  
pin14: +3VA\_H  
pin15: +3VA\_H  
pin16: +3VA\_H  
pin17: +3VA\_H  
pin18: +3VA\_H  
pin19: +3VA\_H  
pin20: +3VA\_H  
pin21: +3VA\_H  
pin22: +3VA\_H  
pin23: +3VA\_H  
pin24: +3VA\_H  
pin25: +3VA\_H  
pin26: +3VA\_H  
pin27: +3VA\_H  
pin28: +3VA\_H  
pin29: +3VA\_H  
pin30: +3VA\_H  
pin31: +3VA\_H  
pin32: +3VA\_H  
pin33: +3VA\_H  
pin34: +3VA\_H  
pin35: +3VA\_H  
pin36: +3VA\_H  
pin37: +3VA\_H  
pin38: +3VA\_H  
pin39: +3VA\_H  
pin40: +3VA\_H  
pin41: +3VA\_H  
pin42: +3VA\_H  
pin43: +3VA\_H  
pin44: +3VA\_H  
pin45: +3VA\_H  
pin46: +3VA\_H  
pin47: +3VA\_H  
pin48: +3VA\_H  
pin49: +3VA\_H  
pin50: +3VA\_H  
pin51: +3VA\_H  
pin52: +3VA\_H  
pin53: +3VA\_H  
pin54: +3VA\_H  
pin55: +3VA\_H  
pin56: +3VA\_H  
pin57: +3VA\_H  
pin58: +3VA\_H  
pin59: +3VA\_H  
pin60: +3VA\_H  
pin61: +3VA\_H  
pin62: +3VA\_H  
pin63: +3VA\_H  
pin64: +3VA\_H  
pin65: +3VA\_H  
pin66: +3VA\_H  
pin67: +3VA\_H  
pin68: +3VA\_H  
pin69: +3VA\_H  
pin70: +3VA\_H  
pin71: +3VA\_H  
pin72: +3VA\_H  
pin73: +3VA\_H  
pin74: +3VA\_H  
pin75: +3VA\_H  
pin76: +3VA\_H  
pin77: +3VA\_H  
pin78: +3VA\_H  
pin79: +3VA\_H  
pin80: +3VA\_H  
pin81: +3VA\_H  
pin82: +3VA\_H  
pin83: +3VA\_H  
pin84: +3VA\_H  
pin85: +3VA\_H  
pin86: +3VA\_H  
pin87: +3VA\_H  
pin88: +3VA\_H  
pin89: +3VA\_H  
pin90: +3VA\_H  
pin91: +3VA\_H  
pin92: +3VA\_H  
pin93: +3VA\_H  
pin94: +3VA\_H  
pin95: +3VA\_H  
pin96: +3VA\_H  
pin97: +3VA\_H  
pin98: +3VA\_H  
pin99: +3VA\_H  
pin100: +3VA\_H



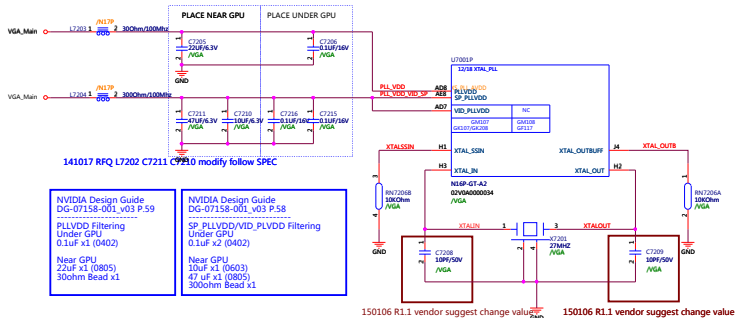
PEGATRON		Title: IO BOARD CON	
DESIGNATION: PROPRIETARY AND CONFIDENTIAL			
REVISION: 1.0			
Project Name		GL553VD	
Date: Monday, September 19, 2011		Sheet 26 of 100	



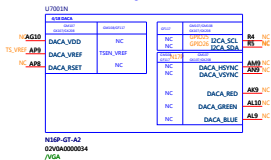




VGA\_Main 57,70,71,74,75,81  
+1.0V5\_VGA 57,70,85

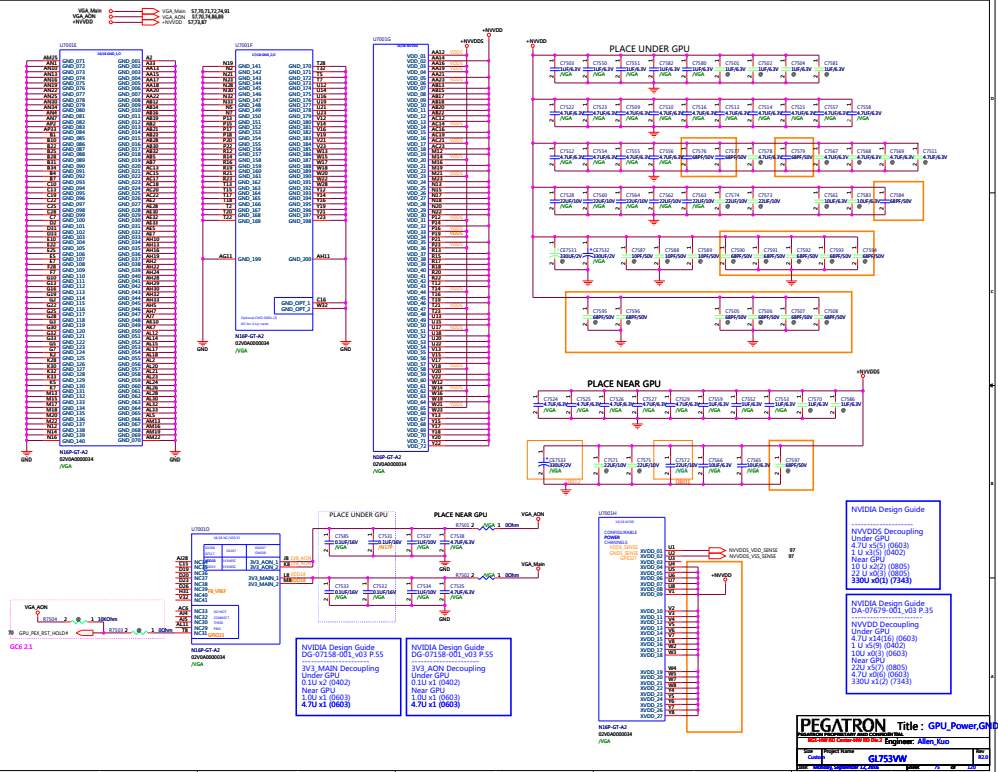


CRT





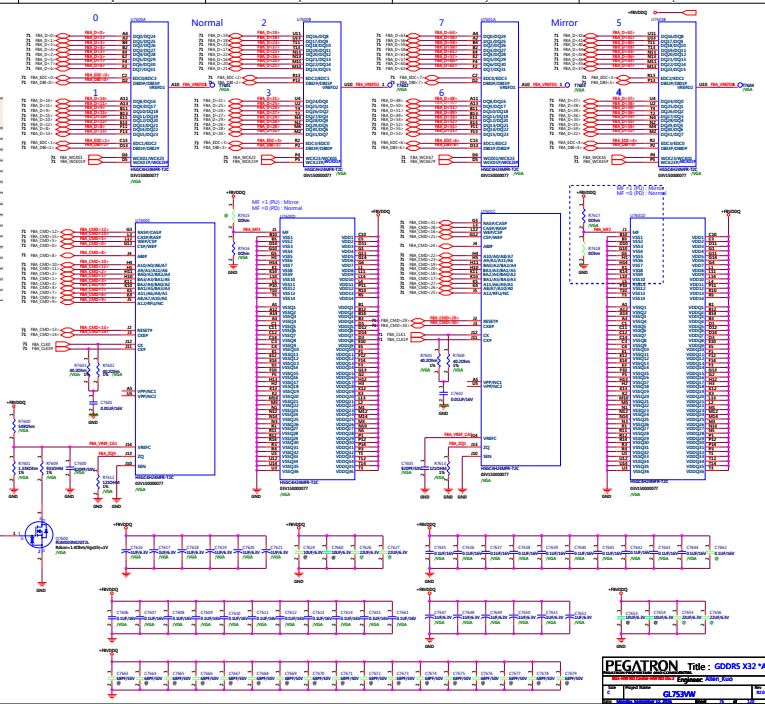




MEMORY: FBA Partition 31.0 (Normal)  
MEMORY: FBA Partition 61.2 (Mirror)

# **DDR5 Mode H Mapping**

GB28-64	CMD0-6-31	GB28-64	CMD1-32-43
GB48-128	GB48-128	GB48-128	
CMD0	C8*	CMD16	C8*
CMD1	A3 BA3	CMD17	A3 BA3
CMD2	A3 BA0	CMD18	A3 BA0
CMD3	A4 BA2	CMD19	A4 BA2
CMD4	A5 BA1	CMD20	A5 BA1
CMD5	W8*	CMD21	W8*
CMD6	A7-48	CMD22	A7-48
CMD7	A6 A11	CMD23	A6 A11
CMD8	AB*	CMD24	AB*
CMD9	A12 RFU	CMD25	A12 RFU
CMD10	A0 A10	CMD26	A0 A10
CMD11	A1 A9	CMD27	A1 A9
CMD12	BA5*	CMD28	BA5*
CMD13	BA3*	CMD29	BA3*
CMD14	CK*	CMD30	CK*
CMD15	CA5*	CMD31	CA5*





# Skylake-H42\_45W (Non-OPC)

Skylake is	+VCCORE	+VCCOST	+VCCSA
120	100	120	120

R12 & R102 Resistance circuit prod in EE #7  
R12 & R102 Resistance reset in Core VR controller

	R12	R102
VIDALERT#	10 ohm	100 ohm
VIDSClk	50 ohm	45 ohm
VIDSOUT	0 ohm	Empty

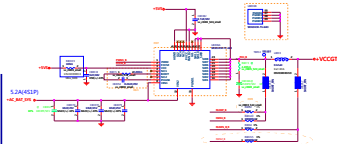
R8039 & R8044 100Kohm

15.8k ohm R series with 100k NTC to trip VR\_HOT# is in 110 deg C  
100 deg C trip VR\_HOT# R series is 14.3k ohm  
120 deg C trip VR\_HOT# R series is 16.9k ohm

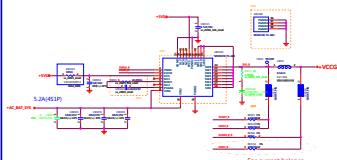
+VCCOST (new) 45W  
VID1: 0.9V  
VID2: 0.9V  
VID3: 0.9V  
Vbatt: 0V  
LL=2.05mohm  
Total Cap: 12.0uF



For current balance

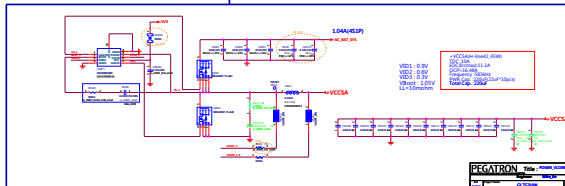
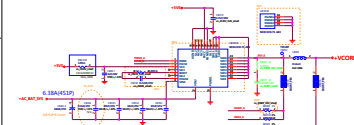
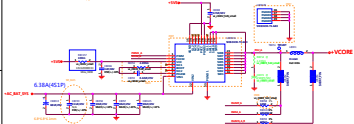
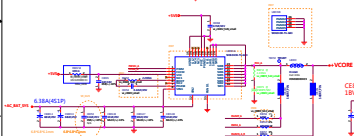


For current balance



CE8000,CE8001,CE8004,CE8007  
1B/080000032(6m ohm)(change to 1B/080000020(2m ohm))

+VCCOST (new) 45W  
VID1: 0.9V  
VID2: 0.9V  
VID3: 0.9V  
Vbatt: 0V  
LL=2.05mohm  
Total Cap: 12.0uF

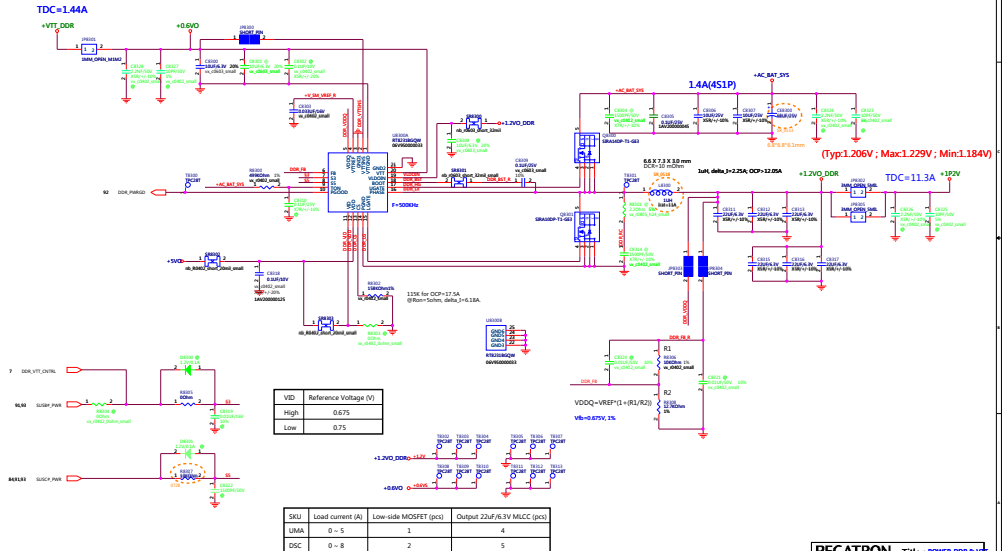


+VCCSA (new) 45W  
VID1: 0.9V  
VID2: 0.9V  
VID3: 0.9V  
Vbatt: 0.9V  
LL=2.05mohm  
Total Cap: 12.0uF





## DDR & VTT POWER SUPPLY





# 1.0VS\_VGA(+1P0V\_GPU) POWER SUPPLY

R8503 need to change Voltage 1V & 1.05V

+1.0VS\_VGA

	N16P-GX	N17P-G1
EDP	2.5A	1.8U
TDC	2.57A	3A
Voltage	1.05V	1V

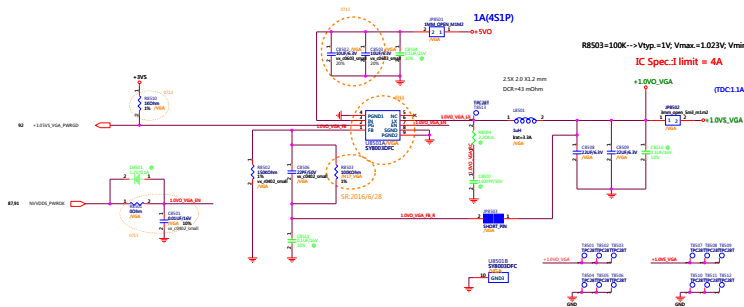
R8503=113K-->Vtyp=1.052V; Vmax=1.077V; Vmin=1.027V

R8503=100K-->Vtyp=1V; Vmax=1.023V; Vmin=0.977V

IC Spec: I limit = 4A

+1.0VS\_VGA

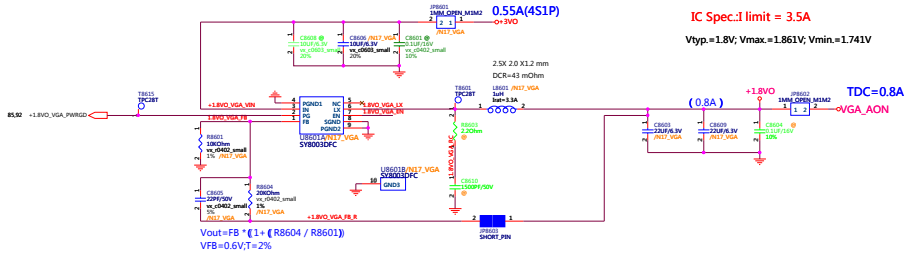
(TDC:1.1A)



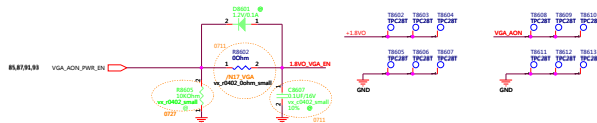
N16P-GX-->VO=1.05V; R8503=113K (10V220000401);  
N17P-G1-->VO=1V; R8503=100K (10V220000004);

Vout=FB \* (1 + (R8503 / R8502))  
VFB=0.6V; T=1.5%

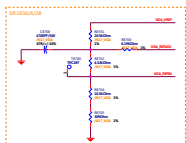
## +1.8V POWER SUPPLY



Frequency:1MHz



# (N17)VGA\_CORE POWER SUPPLY



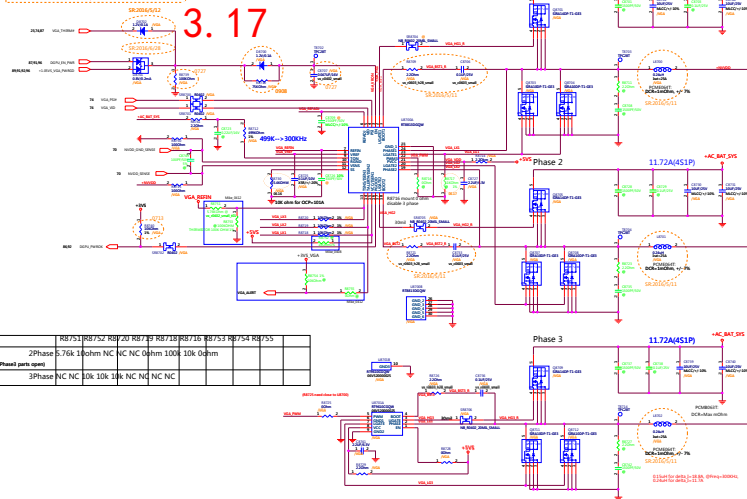
N17P-G0G11 follow DA-67933

Config

R8700	0.15K
R8701	20.5K
R8702	6.52K
R8704	16.5K
R8705	100K
C8700	4.7UF
VDD01	0.5V
VDD04	1.5V
VDD05	0.5V
VSS16	0.500V

VGA_P01	V0 action
1.2 ~ 1.8V	1 Phase VDD01
1.2 ~ 1.8V	2 Phase VDD04
2.4V ~	3 Phase VDD05

3.17



+NVDD			
EDP	N17P-G1	N17P-G0	N16P-GX
TDC	38A	38A	3.2-3.4A

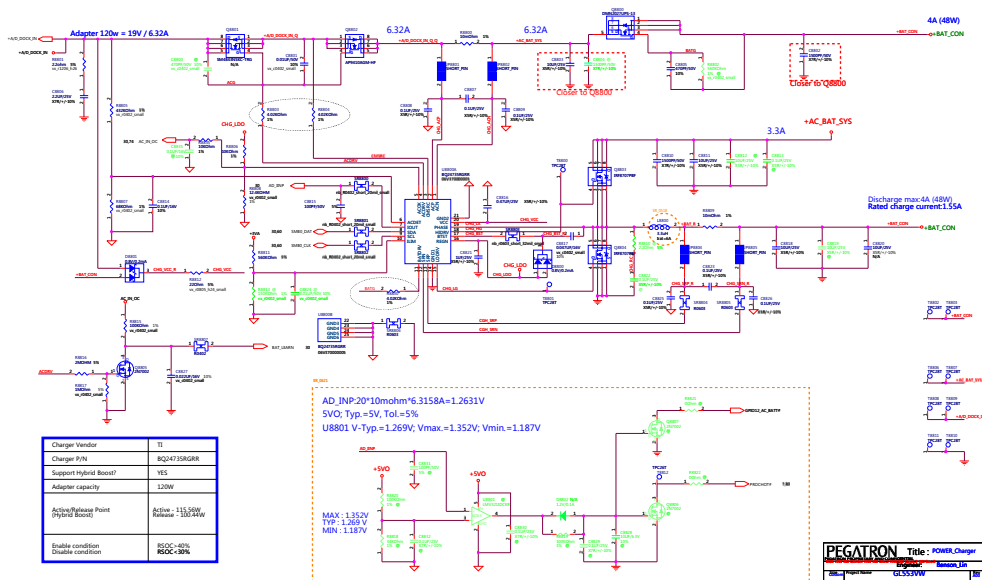
+NVDD  
EDP=101A  
TDC=38A  
OCP100A



EE-N16 ~> (330uF/2V, 6m ohm) \*1pc  
EE-N17 ~> (330uF/2V, 6m ohm) \*2pc

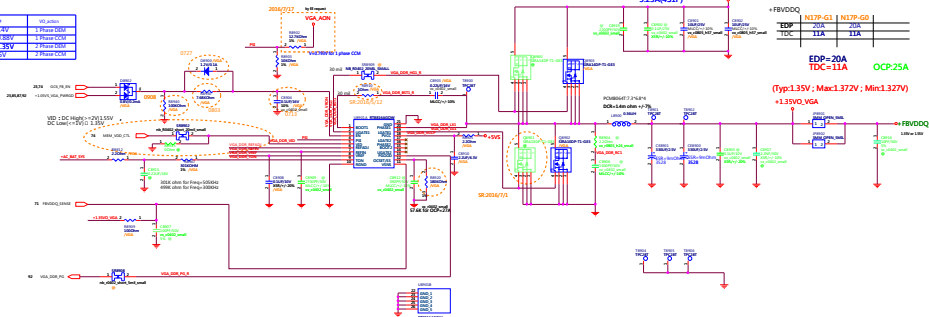


## BATTERY CHARGER



# +FBVDDQ POWER SUPPLY

VGA_P0P	V0_P0P0N
0.9V ~ 1.2V	1.2V ~ 1.8V
0.9V ~ 1.2V	1.2V ~ 1.8V
1.0V ~ 1.3V	1.2V ~ 1.8V
1.0V ~ 1.3V	1.2V ~ 1.8V



+FBVDDQ	
EDP	VGA
TDC	TDC
N17P-G1	N17P-G0
11A	11A

EDP=20A  
TDC=11A

(Typ1.35V; Max1.372V; Min1.327V)

+135VQ\_VGA

+FBVDDQ

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

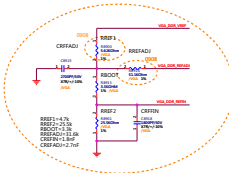
1.35V ~ 1.37V

1.35V ~ 1.37V

1.35V ~ 1.37V

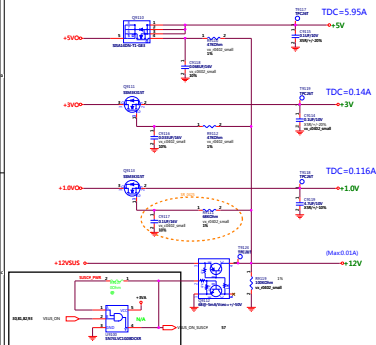
1.35V ~ 1.37V

1.35V ~ 1.37V



MIN_VDDQ_V0	V0
0	1.35V
1	1.37V

# SUSC#\_PWR POWER



ABBA Rule

## SUSB#\_PWR POWER Control



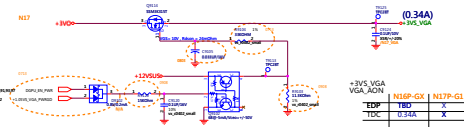
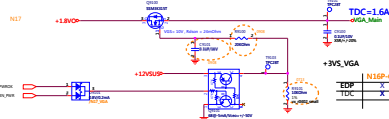
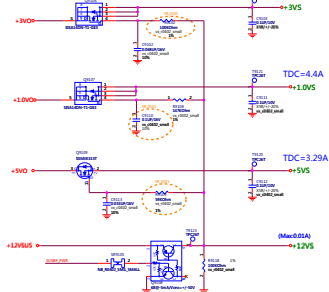
## SUSC#\_PWR POWER Control



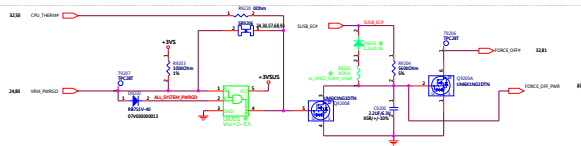
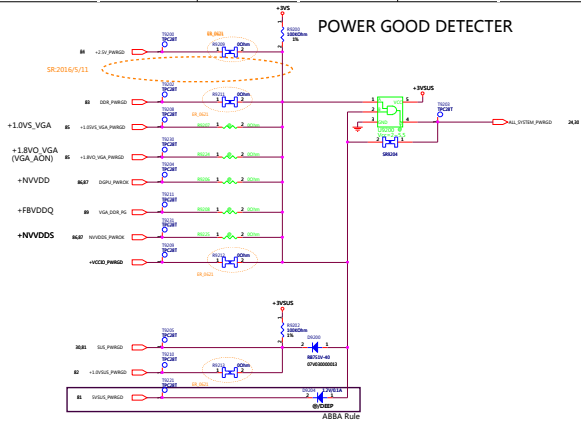
## DSC\_VGA\_PWR POWER Control



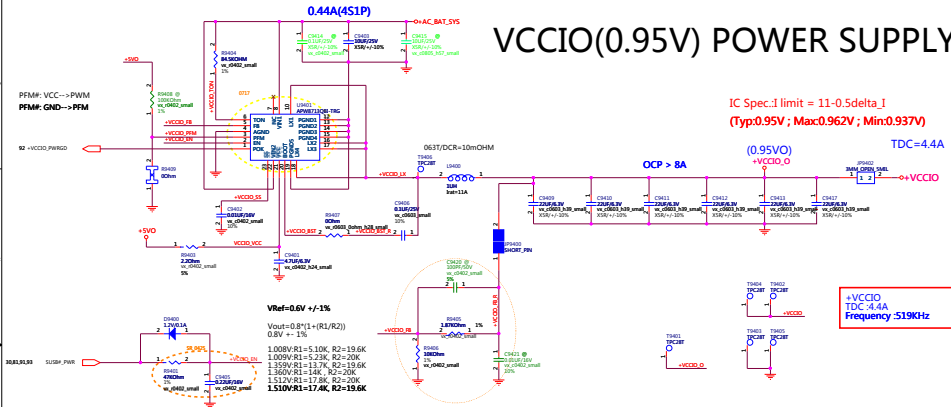
# SUSB#\_PWR POWER



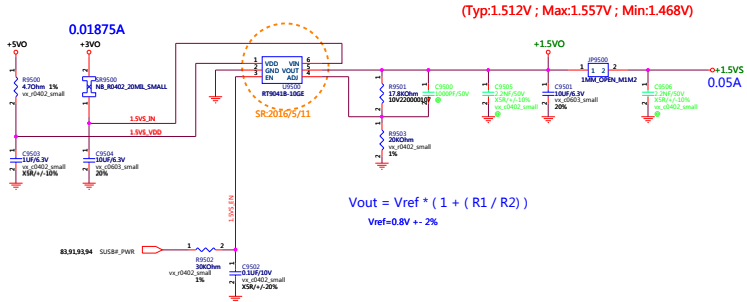
## POWER GOOD DETECTOR



## VCCIO(0.95V) POWER SUPPLY

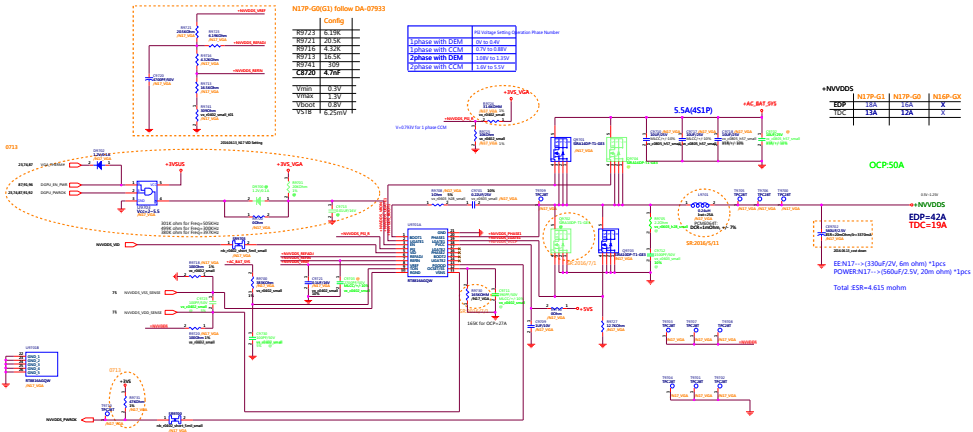


# 1.5V POWER SUPPLY



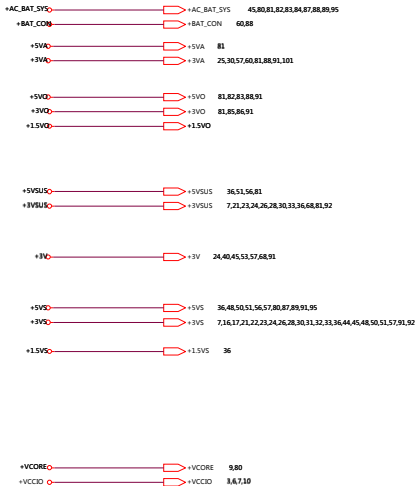
PEGATRON		Title : POWER_1.5VS	
PROJ. NAME: PEGATRON_1.5VS_2016_08_24			
Project Name		GL553VW	Rev
Date		Monday, September 12, 2016	24
Author		Benson_Lin	24

## +NVVDDS POWER SUPPLY

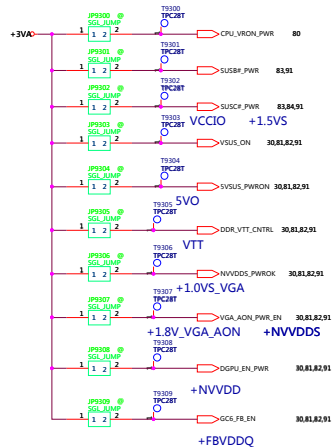








## FOR POWER TEST



<b>PEGATRON</b>		Title : POWER_Signal	
DESIGN ENGINEER		DESIGN ENGINEER	
Engineer		Benson_Lin	
Size	Project Name	GL553VW	800
Monday, September 12, 2016		93	24
Draw	Sheet	of	

# 65.NUT,Screw hole,Tooling hole

## CPU NUT



## GPU NUT



## PCH NUT



## Hall Sensor Brd NUT



## SSD NUT



## NPTH\_2.5phi



## NPTH\_4 x 2.5 phi



## NPTH\_8phi



## NPTH\_2.5 x 2.9 phi



## TYPE A phi 8 drill 3



## TYPE T\_S8 drill3,B\_phi8 drill3 T-SH00004213



## TYPE T\_phi10 drill3,B\_phi8 drill3 ST394CB314D118



## TYPE G T\_9p5 x 8 drill3,B\_phi8 drill3 RT374x314CB314D118



## TYPE phi 6p5 drill 3



## TYPE T\_s8 drill3,B\_R10x8 drill3 RT314RB393x314D118



## TYPE E(BOT) TYPEB(TOP) T\_s8 drill3,B\_R10x8 drill3 RT314RB393x314D118



## TYPE D(BOT) TYPE F(TOP) T\_s7p55 drill3,B\_R10x8 drill3 RT297X315RBD118

